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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/776,541	MORAD ET AL.	
	Examiner	Art Unit	
	Tung Vo	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 February 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02/10/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date ____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 09/10/2008 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 10-20 and 24-33 are rejected under 35 U.S.C. 102(e) as being anticipated by Hinchley (US 6,490,250).

Re claims 10 and 24, Hinchley teaches a single-chip audio/video encoder device (120 of fig. 1) comprising, on a single integrated circuit (fig. 2):

multiplexer circuitry (200 of fig. 2, 750 of fig. 7) that operates in a first mode and a second mode *(Column 6, lines 12-16; Note Hinchley discloses MUX logic 750 which performs*

conventional multiplexing operations in accordance with recognized standards such as MPEG2 to generate the combined (multiplexed) multimedia stream (audio and video) 224, which is similar to the multiplexing circuit as disclosed in paragraph [0063] of the present invention publication (US 2004/0161032 A1)), which when operating in the first mode produces a first multiplexed stream (first combined multimedia stream, 224 of fig. 7) from first compressed video, first compressed audio, second compressed video, and second compressed audio (208 of fig. 2; MPEG-2 standard encoders for encoding video and audio); and which when operating in the second mode concurrently produces the first multiplexed stream (224 of fig. 7) from the first compressed video and the first compressed audio, and produces a second multiplexed stream (224 of fig. 7) from the second compressed video and the second compressed audio (208 of fig. 2; MPEG-2 encoders for encoding the second video and second audio);

a first encoder *(208 of fig. 2, see also fig. 3, the encoder (208 of fig. 2) supports the MPEG-2 standards; col. 3, lines 32-38; which is similar to the encoder of the present invention publication (US 2004/0161032 A1) as shown in paragraph [0036])* that receives first uncompressed video data and first uncompressed audio data (108 of fig. 2), and that produces the first compressed video and the first compressed audio;

a second encoder *(208 of fig. 2; the encoder (208 of fig. 2) supports the MPEG-2 standards; col. 3, lines 32-38; which is similar to the encoder of the present invention publication (US 2004/0161032 A1) as shown in paragraph [0036])* that receives second uncompressed video data and second uncompressed audio data (108 of fig. 2), and that produces the second compressed video and the second compressed audio;

control circuitry *(250 of fig. 2, the multimedia processor is designed to perform multimedia operations as well as specialized functions, which is similar to the global controller (104) of the present invention publication (US 2004/0161032 A1) as shown in paragraph [0050]; the MPEG-2 inherently has the control function to synchronize the multiplexer, audio and video encoder together, since Hinchley discloses MUX logic 750 which performs conventional multiplexing operations in accordance with recognized standards such as MPEG2 to generate the combined (multiplexed) multimedia stream (audio and video) 224 and controller 250 for synchronize the multiplexer, and audio and video encoders according to the MPEG-2 standards))* that synchronizes ***(harmonizes, coordinates, or orchestrates)*** the multiplexing circuitry (200 of fig. 2; col. 7), the first encoder, and the second encoder (208 of fig. 2);

wherein the device (120 of fig. 2) transmits the first multiplexed stream (224 of fig. 2; col. 6, lines 6, lines 18-26) to circuitry external (e.g. 104, 128, 112, and 116 of fig. 1) to the device via a first output of the device; and wherein the device transmits the second multiplexed stream (224 of fig. 2) to circuitry external (116 of fig. 1) to the device via a second output of the device.

Re claim 11, Hinchley further discloses wherein the first encoder and the second encoder each comprise a video encoder and an audio encoder (col. 10, lines 10-24).

Re claims 12 and 25, Hinchely further discloses wherein the first encoder and the second encoder operate concurrently (208 of fig. 2).

Re claims 13 and 26, Hinchely further discloses wherein the first encoder and the second encoder inherently perform luminance and chrominance filtering *(note MPEG-1 and MPEG-2 video/audio compression standards. Hence, a data block represents a macroblock, which is a*

sixteen by sixteen matrix of luminance pixels and two, four or eight, by eight matrices of chrominance pixels as defined by MPEG standards, wherein luminance and chrominance are 4:2:0, 4:2:2, or 4:4:4 as shown in Hinchley, col. 3, lines 30-38).

Re claims 14 and 27, Hinchley further discloses wherein the device comprises at least one interface (122 of fig. 1) for direct connection to external memory devices (108 and 116 of fig. 1) used as one or both of a frame buffer and/or an output buffer for compressed data.

Re claims 15 and 28, Hinchley further discloses wherein the device comprises at least one bus interface (122 of fig. 1) that is configurable to operate to couple the control circuitry (250 of fig. 1) and at least one controller external (104 of fig. 1) to the device,

wherein the at least one bus interface (122 of fig. 1) comprises inherently a plurality of separate electrical signals *(note each of the components inherently has its own electrical signal (e.g. electron, voltage, digital data). Figure 1 of Hinchley has a plurality of separate electrical elements that inherently have a plurality of separate electrical signals. It is further noted that the specification of the present invention does not particularly disclose a plurality of separate electrical signals, so the plurality of electrical signals are understood that each element has its own electrical signal as shown in fig. 1 of Hinchley, e.g. the integrated multimedia encoding system has its own electrical signal (e.g. encoded data, uncompressed data ...)).*

Re claims 16 and 29, Hinchley further discloses wherein the at least one bus interface is configurable as a peripheral component interconnect (PCI) bus interface *(Note Hinchley teaches the unified memory module 204 receives the adjusted elementary streams 216, 218, the output combined data 224 as well as data streams from other data sources 236, such as from the PCI bus, through a conventional FIFO 244).*

Re claims 17 and 30, Hinchley further discloses wherein the at least one bus interface is configurable to act as a bus master (122 of fig. 1) inherently using direct memory access *(support by Larson, US 5,821,987, the vision processor 48B preferably incorporates a DMA data interface with a zero-run/amplitude encoder/decoder, fig. 1).*

Re claims 18 and 31, Hinchley further discloses wherein the at least one bus interface (122 of fig. 1) enables transfer of one or both of uncompressed audio data and/or video data for processing by the device.

Re claims 19 and 32, Hinchley further discloses wherein the first encoder, the second encoder, and the multiplexer circuitry execute microcode instructions *(e.g. 104 of fig. 1; note the computer system 100 has a central processing unit 104, which may execute specific programs related to multimedia processing; wherein a program inherently has microcode instructions, e.g. 606 of fig. 6; col. 5, lines 25-65)* received by the device via the at least one bus interface (122 of fig. 1, PCI bus).

Re claims 20 and 33, Hinchley further discloses wherein each of the first uncompressed audio data and the second uncompressed audio data represent two audio channels (108 of fig. 1).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 21-22 and 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hinchley et al. (US 6,490,250) in view of Ishihara et al. (US 6,516,031).

Re claims 21-22 and 34-35, Hinchely teaches the MPEG-2 encoder (208 of fig. 2) that would obviously has motion estimation except a plurality of search processors for performing motion analysis in parallel, each upon a different portion of a macroblock as claimed.

However, Ishihara teaches a plurality of search processors (7 of fig. 2) for performing motion analysis in parallel, each upon a different portion of a macroblock (PE1, PE2....PE33 of fig. 7; e.g. fig. 13).

Taking the teachings of Hinchley and Ishihara as a whole, it would have been obvious to one of ordinary skill in the art to modify the processor array (7 of fig. 2) of Ishihara into the motion estimation of Hinchley to provide an improvement for reducing a hardware volume.

6. Claims 23 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hinchley et al. (US 6,490,250) in view of Ishihara et al. (US 6,516,031) and further in view of Kopet et al. (US 5,448,310).

Re claim 23, the combination of Hinchley and Ishihara further teaches wherein the plurality of search processors operates in parallel upon a single macroblock (e.g. figs. 9 and 10 of Ishihara) and suggests the processor performs half pixels search, except each search processor operating at a different one of a plurality of resolutions as claimed.

However, Kopet teaches the motion estimation coprocessor of the present invention provides improvements in performance over prior art devices. For example, the motion estimation coprocessor of the present invention may perform either full, exhaustive block

matching searches or multiple step hierarchical searches to either full or half pixel search resolution (col. 2, line 50 –col. 3, line 29).

Taking the teachings of Hinchley, Ishihara, and Kopet as a whole, it would have been obvious to one of ordinary skill in the art to modify the teachings of Kopet into the combined motion estimation of Hinchley and Ishihara in order to improve system speed and performance over prior art devices through parallel performance of these tasks.

7. Claims 10-12, 15-16, 20, 24-25, 28-29, and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnamurthy et al. (US 6,665,872).

Re claims 10 and 24, Krishnamurthy teaches a single-chip audio/video encoder device (fig. 3) comprising, on a single integrated circuit (fig. 3, note two and more different sub-system could be implemented on a single board, col. 20, lines 34-42):

multiplexer circuitry (308 of fig. 3) that operates in a first mode and a second mode (col. 20, lines 22-25, "multi-channel mode" would obviously suggest a first mode and a second mode), which when operating in the first mode (308 of fig. 3, the multiplexer (308) for multiplexing up to 24 different channels of transport bitstreams from the MPEG-2 encoders; col. 20, lines 10-11) produces a first multiplexed stream (fig. 5, multiplexing bitstreams and outputting a first multiplexed bitstream) from first compressed video (320 of fig. 3), first compressed audio (322 of fig. 3), second compressed video (ENCn, 320 of fig. 3), and second compressed audio (ENCn, 322 of fig. 3); and which when operating in the second mode concurrently produces the first multiplexed stream from the first compressed video and the first compressed audio (SSI, 328 of fig. 3), and produces a second multiplexed stream (fig. 5,

multiplexing bitstreams and outputting a second multiplexed bitstream) from the second compressed video and the second compressed audio (AUDIO ENC and MPEG-2 ENC of fig. 3);

a first encoder (306 of fig. 3) that receives first uncompressed video data and first uncompressed audio data, and that produces the first compressed video and the first compressed audio;

a second encoder (306 of fig. 3, ENCn) that receives second uncompressed video data and second uncompressed audio data, and that produces the second compressed video and the second compressed audio;

control circuitry (304 of fig. 3, note the CPU (304) is programmable to control all elements, so the CPU would obviously synchronize all element as described in figure 3) that synchronizes the multiplexing circuitry, the first encoder, and the second encoder;

wherein the device (fig. 3, see also fig. 5) transmits the first multiplexed stream to circuitry external (506 of fig. 5, col. 20, lines 27-28) to the device via a first output of the device; and wherein the device (fig. 5) transmits the second multiplexed stream to circuitry external (506 of fig. 5; col. 20, lines 27-28) to the device via a second output of the device.

Re claim 11, Krishnamurthy further teaches wherein the first encoder and the second encoder each comprise a video encoder and an audio encoder (306, 320, and 322 of fig. 3; ECNn of fig. 3).

Re claims 12 and 25, Krishnamurthy further teaches wherein the first encoder and the second encoder operate concurrently (parallel encoding, 306 of fig. 3).

Re claims 15 and 28, Krishnamurthy further teaches wherein the device comprises at least one bus interface (PCI, 302 and 310 of fig. 3) that is configurable to operate to couple the

control circuitry (304 of fig. 3) and at least one controller external (316 of fig. 3, downloading micro-codes for MPEG-2 encoder chip, 306 of fig. 3, col. 19, lines 22-28) to the device, wherein the at least one bus interface comprises a plurality of separate electrical signals (PCI of fig. 3).

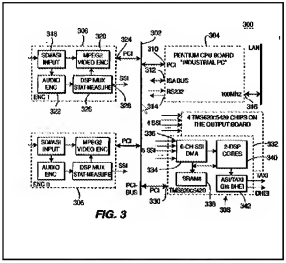
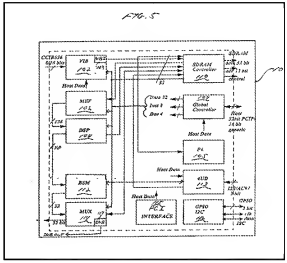
Re claims 16 and 29, Krishnamurthy further teaches wherein the at least one bus interface is configurable as a peripheral component interconnect (PCI) bus interface (302, PCI BUS of fig. 3).

Re claims 20 and 33, Krishnamurthy further teaches wherein each of the first uncompressed audio data and the second uncompressed audio data represent two audio channels (AUDIO ENC of fig.3).

Re claims 18-19, 31-32, Krishnamurthy further teaches wherein the at least one bus interface enables transfer of one or both of uncompressed audio data and/or video data for processing by the device (318 of fig. 3); wherein the first encoder, the second encoder, and the multiplexer circuitry execute microcode instructions received by the device via the at least one bus interface ("C" programmable language and micro-codes are used to instruct elements in figure 3; col.18, lines 28-33; col. 19, lines 26-28).

The arguments in the remarks filed on 09/10/2008, the applicant argues that the Office Action fails to identify any portion of text of Krishnamurthy teaches "multiplexing circuit" for operating in a first mode and second mode, the first multiplexed stream coupled via the fist output to circuitry external to the device, a second multiplexed stream coupled to via second output to circuitry external to the device, single chip video/audio encoder device, the controller circuitry synchronizes operation of the first encoder circuitry, the second encoder circuitry, and the multiplexer circuitry in the remarks.

The examiner respectfully disagrees with the applicant. It is submitted that Krishnamurthy teaches a single audio/video encoder device (fig. 3) that is similar to the described single audio/video device of the present invention as follows:

Krishnamurthy	The present invention
	

Krishnamurthy teaches a first MPEG-2 video encoder (320), a first audio encoder (322), a second MPEG-2 encoder (320n, 306n), a second audio encoder (322n, 306n), and a statistical multiplexing board (308), wherein the statistical multiplexing board (308 of fig. 3) is a multiplexing circuit for multiplexing the first encoded video signal and the first encoded audio signal (SSI, 328, 336), and the second encoded video signal and the second encoded audio signal (SSI, 328n, 336). The stat-mux (308 of fig. 3) can multiplex up to 24 channels of low delay MPEG-2 video/audio input bitstreams (SSI of fig. 3, col. 18, lines 50-52; col. 20, lines 10-11); and each SSI has three wires carrying a clock signal (sclk), a data signal (sdat), and a frame signal (col. 20, lines 12-13), and the frame signals can also be programmed in a "multi-channel mode" to send multiple packets into assigned on-chip buffers for transmitting the individual

encoders' statistical parameters (col. 20, lines 22-25), so this is evidence to one of ordinary skill in the art to modify the stat-mux (308) of Krishnamurthy within a single chip for multiplexing the first encoded video and audio in a first mode and the second encode video and audio in a second mode.

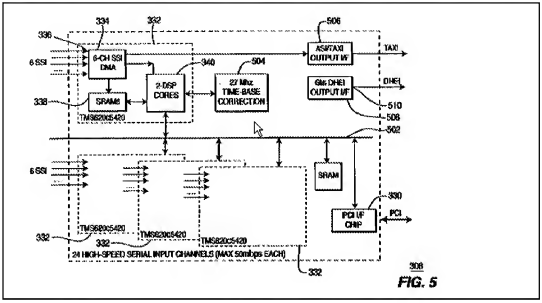


FIG. 5

Krishnamurthy further teaches the stat-mux in figure 5 for outputting the multiplexed stream of the first encoded video and the first encoded video to circuitry external to the device (506, col. 20, lines 27-28), wherein the stat-mux (308 of fig. 5) would obviously output the multiplexed stream of the second encoded video and the second encoded audio to circuitry external to the device (506; col. 20, lines 27-28) via "TAXI", which is similar to the MUX (114 of fig. 5) of the present invention.

Krishnamurthy further teaches a Central Processing Unit (CPU) (304 of fig. 3) that is programmable to control all elements in the circuit board of figure 3, so the Central Processing Unit (CPU) (304 of fig. 3) would synchronize, coordinate, or harmonize all operations of the first

encoder circuitry (306 of fig. 3), the second encoder circuitry (306n of fig. 3), and the multiplexer circuitry (308 of fig. 3) in order for all circuits properly working. Since Krishnamurthy teaches the MPEG-2 encoder chip that would obviously has a control function to synchronize the multiplexer, audio and video encoders according the MPEG-2 standards, therefore one of ordinary skill in the art to modify the control function according to MPEG-2 into the CPU (304 of fig. 3) to perform synchronization. In view of the discussion above, the claimed features are unpatentable over Krishnamurthy.

In response to applicant's argument of the obviousness, the examiner would like point out the following basic principle of a proper prior art analysis within 35 U.S.C. 103 (a).

Not only the specific teachings of a reference but also reasonable inferences which the artisan would have logically drawn therefrom may be properly evaluated in formulating a rejection. In re Preda, 401 F.2d 825, 159 USPQ 342 (CCPA 1968) and In re Shepard, 319 F.2d 194, 138 USPQ 148 (CCPA 1963). Skill in the art is presumed. In re Sovish, 769 F.2d 738, 226 USPQ 771 (Fed. Cir. 1985). Furthermore, artisans must be presumed to know something about the art apart from what the references disclose. In re Jacoby, 309 F.2d 513, 135 USPQ 317 (CCPA 1962).

The obviousness may be made from common knowledge and common sense of a person of ordinary skill in the art without any specific hint or suggestion in a particular reference. In re Bozek, 416 F.2d 1385, 163 USPQ 545 (CCPA 1969)). Every reference relies to some extent on knowledge of persons skilled in the art to complement that which is disclosed therein. In re Bode, 550 F.2d 656, 193 USPQ 12 (CCPA 1977).

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the

teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the Office Action above, paragraph 9, suggests all limitations to make obvious the claimed invention.

8. Claims 13 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnamurthy et al. (US 6,665,872) in view of Bruck (US 6,519,289).

Re claims 13 and 26, Krishnamurthy does not particularly teach wherein the first video encoder and the second video encoder perform luminance and chrominance filtering.

However, Bruck teaches wherein the video encoder performs luminance and chrominance filtering (col. 1, lines 59-col. 2, line 8).

Taking the teachings of Krishnamurthy and Bruck as a whole, it would have been obvious to one of ordinary skill in the art to modify the luminance and chrominance filtering of Bruck into Krishnamurthy to improve the picture quality.

In response to the applicant arguments filed on 06/10/2008, the applicant argues that Bruck fails to overcome the deficiencies of Krishnamurthy, page 23.

The examiner respectfully disagrees with the applicant. It is submitted that Krishnamurthy teaches the encoder (306 of fig. 3) for encoding video and audio stream based on the MPEG-2 standards, wherein the MPEG-2 standard would obviously have the luminance and

chrominance filtering by Bruck (col. 1, lines 59-col. 2, line 8). Therefore, the combination of Krishnamurthy and Bruck make obvious the claimed invention.

9. Claims 14, 17-19, 27, 30-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnamurthy et al. (US 6,665,872) in view of Hinchley et al. (US 6,490,250).

Re claims 14, 17, 27, and 30 , Krishnamurthy does not particularly disclose external memory devices used as one or both of a frame buffer and/or an output buffer for compressed data; wherein the at least one bus interface is configurable to act as a bus master using direct memory access as claimed.

Hinchley teaches a first storage external to the device and a second storage external (108 and 116 of fig. 1) to the device (120 of figs. 1 and 2) and the at least one bus interface is configurable to act as a bus master (122 of fig. 1) using direct memory access (Note the bus (122) would obviously be the PCI bus and/or direct memory access, which serves the same purpose of transferring and receiving data to and from components within the circuit (100 of fig. 1).

Therefore, taking the teachings of Krishnamurthy and Hinchley, it would have been obvious to one of ordinary skill in the art to incorporate the first and second storages and random access memory with the interface bus (108, 116, and 122 of fig. 1) of Hinchley into the first and second interface (318 of fig. 2) Krishnamurthy to provide an integrated multimedia encoding system which operates with reduced memory storage requirements is also needed.

Re claims 18-19, 31-32, Krishnamurthy further teaches wherein the at least one bus interface (PCI BUS, 302 of fig. 3) enables transfer of one or both of uncompressed audio data

and/or video data for processing by the device (318 of fig. 3); wherein the first encoder, the second encoder, and the multiplexer circuitry execute microcode instructions received by the device via the at least one bus interface ("C" programmable language and micro-codes are used to instruct elements in figure 3; col.18, lines 28-33; col. 19, lines 26-28).

10. Claims 21-22 and 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnamurthy et al. (US 6,665,872) in view of Boice et al. (US 6,823,013).

Re claims 21-23, and 34-36, Krishnamurthy does not particularly disclose each of motion estimation processors comprises a plurality of search processors that operate in parallel upon a single macroblock, and each search processor operating at a different one of a plurality of resolutions (scaling or half pixel search, quarter pixel search) as claimed.

Boice teaches each of motion estimation processors (52 of fig. 4) comprises a plurality of search processors (see Abstract: a consequence of the multiple processors subdividing the extended window and analyzing each subdivision in parallel) that operate in parallel upon a single macroblock (figs. 1 and 3), and each search processor operating at a different one of a plurality of pixels blocks (scaling or half pixel search, quarter pixel search, 36, 38, and 40 of fig. 3)

Therefore, taking the teachings of Krishnamurthy and Boice as a whole, it would have been obvious to one of ordinary skill in the art to incorporate the plurality of search processors (52 of fig. 4) of Boice into each of motion estimation processor of Krishnamurthy to provide the process of motion estimation effectively reduces the temporal redundancy in successive video

frames by exploiting the temporal correlation (similarities) that often exists between successive frames.

11. Claims 21-22 and 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnamurthy et al. (US 6,665,872) in view of Boice et al. (US 6,823,013) further in view of further in view of Kopet et al. (US 5,448,310).

Re claim 23, the combination of Krishnamurthy and Boice teaches wherein the plurality of search processors operates in parallel upon a single macroblock, except each search processor operating at a different one of a plurality of resolutions as claimed.

However, Kopet teaches the motion estimation coprocessor of the present invention provides improvements in performance over prior art devices. For example, the motion estimation coprocessor of the present invention may perform either full, exhaustive block matching searches or multiple step hierarchical searches to either full or half pixel search resolution (col. 2, line 50 –col. 3, line 29).

Taking the teachings of Krishnamurthy, Boice, and Kopet as a whole, it would have been obvious to one of ordinary skill in the art to modify the teachings of Kopet into the combined motion estimation of Krishnamurthy and Boice in order to improve system speed and performance over prior art devices through parallel performance of these tasks.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Boice et al. (US 7,072,393) discloses multiple parallel encoders and statistical analysis thereof for encoding a video sequence.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tung Vo whose telephone number is 571-272-7340. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mehrdad Dastouri can be reached on 571-272-7418. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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/Tung Vo/
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